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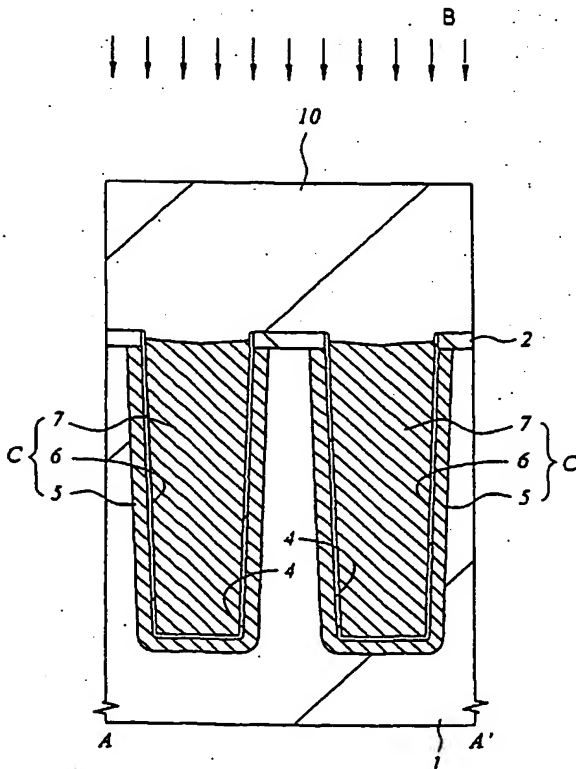
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(54) Title: LONGITUDINAL MISFET MANUFACTURING METHOD, LONGITUDINAL MISFET, SEMICONDUCTOR STORAGE DEVICE MANUFACTURING METHOD, AND SEMICONDUCTOR STORAGE DEVICE

(54) 発明の名称: 縦型 MISFET の製造方法、縦型 MISFET、半導体記憶装置の製造方法および半導体記憶装置



(57) Abstract: When manufacturing a semiconductor storage device including a longitudinal MISFET having a source region, a channel forming region, a drain region, and a gate electrode formed on a side wall portion of the channel forming region via a gate insulation film, boron which is a reverse-conductive with respect to phosphor diffused in a polycrystal silicon film (10) constituting the channel forming region is counterdoped from the n-type polycrystal silicon film (7) constituting the source region of the longitudinal MISFET to the aforementioned polycrystal silicon film (10). This reduces effective impurities concentration in the polycrystal silicon film (10), thereby realizing a longitudinal MISFET having little leak current (off current).

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添付公開書類:

— 国際調査報告書

2文字コード及び他の略語については、定期発行される各PCTガゼットの巻頭に掲載されている「コードと略語のガイダンスノート」を参照。

(57) 要約:

ソース領域、チャネル形成領域およびドレイン領域と、前記チャネル形成領域の側壁部にゲート絶縁膜を介して形成されたゲート電極とを有する縦型MISFETを備えた半導体記憶装置を製造する際、縦型MISFETのソース領域を構成するn型の多結晶シリコン膜(7)からチャネル形成領域を構成する多結晶シリコン膜(10)に拡散するリンとは逆導電型のホウ素を上記多結晶シリコン膜(10)にカウンタードープし、多結晶シリコン膜(10)の実効的な不純物濃度を低減することによって、リーク電流(オフ電流)の少ない縦型MISFETを実現する。

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Int.Cl⁷ H01L21/8242, H01L27/108, H01L29/78

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Kokai Jitsuyo Shinan Koho	1971-2003	Jitsuyo Shinan Toroku Koho	1996-2003
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Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP02/10510

(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>US 5670803 A (International Business Machines Corp.), 23 September, 1997 (23.09.97), All drawings & JP 8-241931 A All drawings & KR 188623 B</p>	<p>3, 7, 12, 16, 23-27, 31, 32, 51, 55-60, 63, 64</p>
	& US 6174763 B	

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP02/10510

Box I Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

☐ Claims Nos.:

because they relate to subject matter not required to be searched by this Authority, namely:

1. ☐ Claims Nos.:

because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:

because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

As is described on the extra sheet, in order to satisfy the requirement of unity of invention, a special technical feature is required to link the inventions disclosed in the claims as to form a single general inventive concept. However, the present international application includes six groups of inventions: claims 1, 2, 4-13, claim 3, claims 14, 15, claims 16, 22-32, claims 17-21, 33-50, and claims 51-64.

(Continued to extra sheet)

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest ☒ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP02/10510

Continuation of Box No.II of continuation of first sheet(1)

Document 1: JP 63-29571 A (Hitachi Ltd.), 1988.02.08
Document 2: US 5821579 A (LG Semicon C., Ltd.), 1998.10.13
Document 3: US 5670803 A (International Business Machines Corporation), 1997.09.23

The technical feature common to claims 1 to 64 is configuration of "having a gate electrode formed on a side wall of the channel forming region via the gate insulation film".

However, the search has revealed that the configuration of "having a gate electrode formed on a side wall of the channel forming region via the gate insulation film" is not novel since it is disclosed in all the drawings of Document 1, Figures 2 to 4 of Document 2, and all the drawings of Document 3.

As a result the configuration of "having a gate electrode formed on a side wall of the channel forming region via the gate insulation film" makes no contribution over the prior art and cannot be a special technical feature within the meaning of PCT Rule 13.2, second sentence.

Consequently, there is no technical feature common to all the claims.

Since there exists no other common feature which can be considered as a special technical feature within the meaning of PCT Rule 13.2, second sentence, no technical relationship within the meaning of PCT Rule 13 between the different inventions can be seen.

Therefore, it is obvious that claims 1 to 64 do not satisfy the requirement of unity of invention.

(1) The independent claims 1, 2, 4, 5 have a special technical feature common to them that "a thermal treatment step" is performed after formation of an intermediate semiconductor layer in the longitudinal MISFET manufacturing method.

(2) The independent claim 3 relates to a longitudinal MISFET manufacturing method but has no special technical feature since the method is disclosed in the aforementioned Documents 1 to 3.

(3) The independent claim 14 has a special technical feature that in the longitudinal MISFET "the impurities concentration inserted into the intermediate semiconductor layer is low in the region nearer to the lower semiconductor layer and the upper semiconductor layer and high in the region far from the lower semiconductor layer and the upper semiconductor layer".

(4) The independent claim 16 relates to a semiconductor storage device manufacturing method but has no special technical feature since the method is disclosed in the aforementioned Documents 1 to 3.

(5) The independent claims 17, 18, 19, 20, and 21 have a special technical feature common to them that "a thermal treatment step" is performed after formation of the channel formation region in the semiconductor storage device manufacturing method.

(6) The independent claims 51, 63, 64 relate to a semiconductor storage device but has no special technical feature since the device is disclosed in the aforementioned Documents 1 to 3.

Consequently, the present international application includes six inventions.